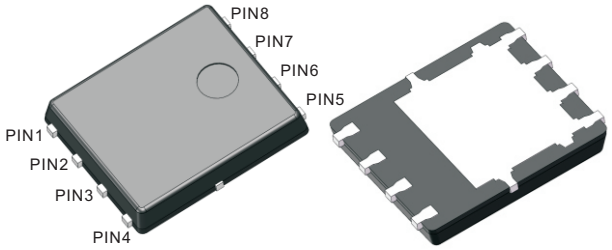
100A, 40V N-CHANNEL POWER MOSFET

PDFN5060-8L(*Prefix :L)



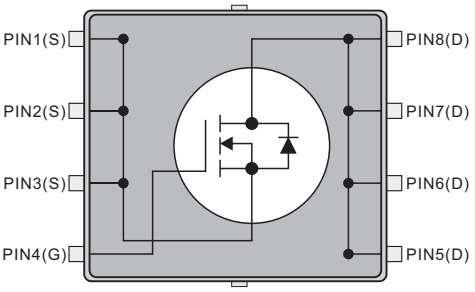
Description

This model is an n-channel enhanced MOS power field effect transistor manufactured by silicon epitaxial process. This model has excellent switching characteristics, extremely low on impedance, low gate charge and other characteristics.

Features

- Hireliability application and automotive grade AEC-Q101 qualified
- Moisture sensitivity level 1
- $R_{DS(ON)}$ < 2.1 mΩ @ V_{GS}=10V, I_D=50A
- Extremely low on impedance
- Low gate charge
- Superior switching characteristics
- 100% Avalanche tested
- 100% △V_{DS} tested

Automotive Grade



S:Source
G:Gate
D:Drain

RoHS COMPLIANT

Mechanical data

- Case: PDFN5060-8L
- Approx. Weight:0.093g (0.0032oz)
- Lead free finish, RoHS compliant
- Case Material: “Green” molding compound, UL flammability classification 94V-0,“Halogen-free”.

Packing Marking And Ordering Information

Device Package	Device	Marking	Packing Type	QTY Per Reel	Inner box	Per Carton
PDFN5060-8L	L1R7NS40S	L1R7NS40S	Reel	5,000 Pcs	10,000 Pcs	50,000 Pcs

Absolute Maximum Ratings (Ta=25°C, Unless Otherwise Specified)

Parameter	Symbols	Ratings	Units
Drain-Source Voltage	V_{DSS}	40	V
Gate-Source Voltage	V_{GSS}	±20	V
Continuous Drain Current V_{GS}=10V,Tc=25℃	I_D	100	A
Pulsed Drain Current Tc=25 °C	I_{DM}	400	A
Avalanche energy, single pulse(Note1)	E_{AS}	264	mJ
Power dissipation Tc=25 °C	P_{tot}	83	W
Operating junction and storage temperature	T_j,T_{stg}	-55 ~ +150	°C

Thermal Characteristics

Parameter		Symbols	Ratings	Units
Device on PCB cooling area (Note2)		R_{thJA}	50	°C/W
Thermal resistance, junction - case	Bottom	R_{thJC}	1.5	°C/W
	Top		18	

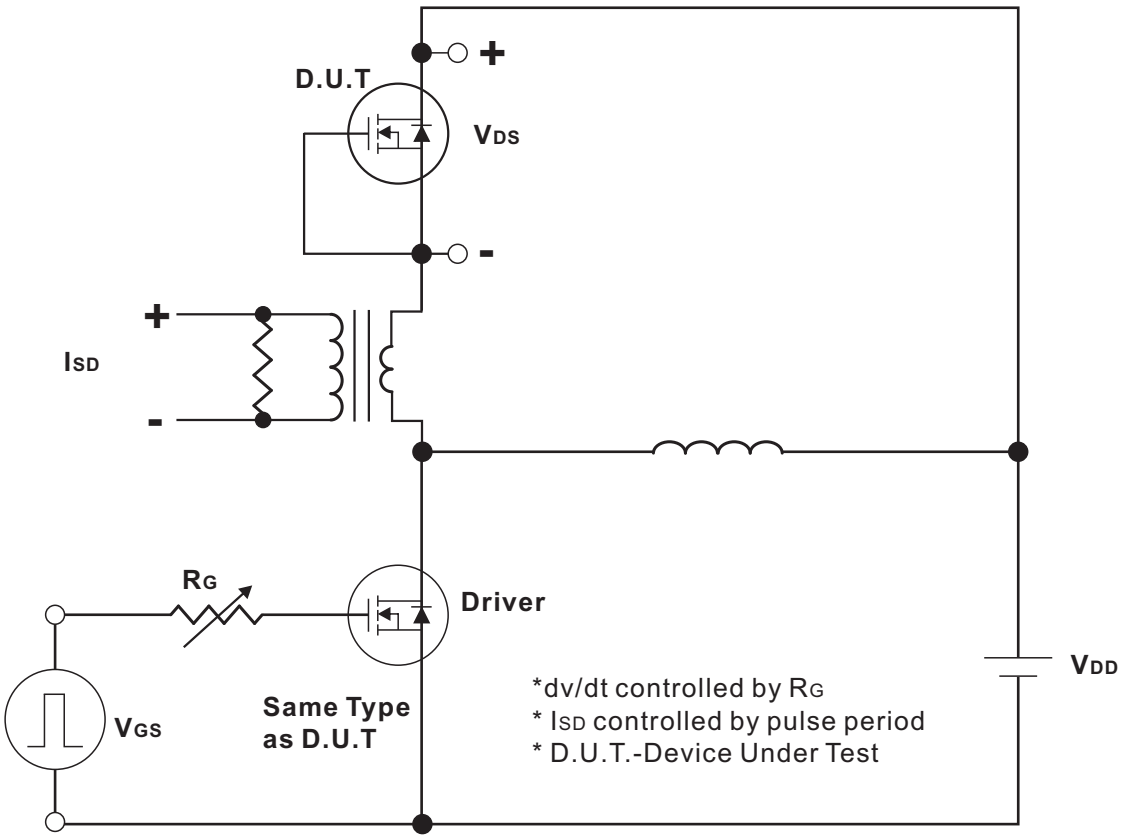
NOTE:
1.L = 0.5mH, I_D =32.5A, R_G = 25 Ω, Starting T_J = 25°C
2.Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR-4 with 6 cm2 (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

Electrical Characteristics (Ta=25°C, Unless Otherwise Specified)

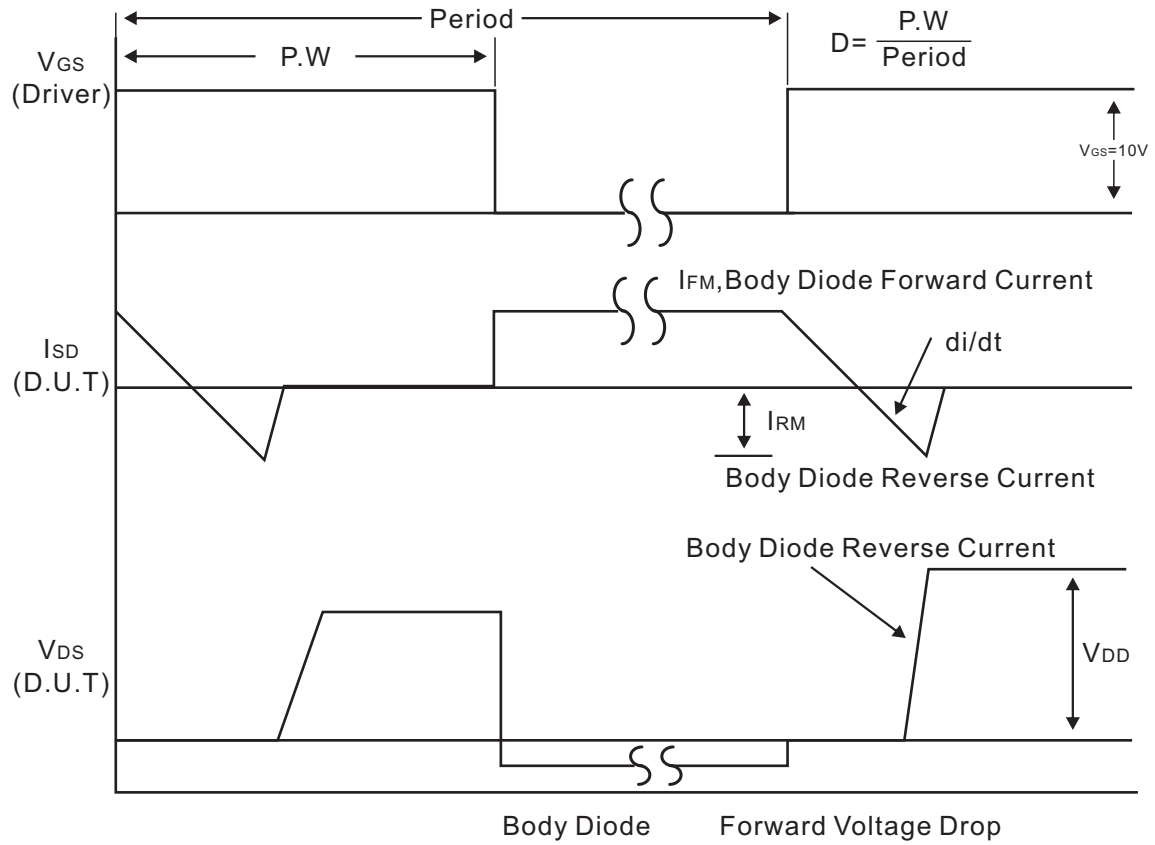
Parameter	Symbols	Test conditions	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250uA	40			V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V		0.1	1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=20V,V_{DS}=0V		10	100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250uA	1.4		2.4	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V,I_D=50A		2.4	3.0	mΩ
		V_{GS}=10V,I_D=50A		1.7	2.1	
Gate resistance	R_G			1.6		Ω
Transconductance	g_{fs}	V_{DS}=5V,I_D=50A		60		S
Dynamic Characteristics						
Input Capacitance	C_{ISS}	V_{DS}=20V,		4766		pF
Output Capacitance	C_{OSS}	V_{GS}=0V,		1821		pF
Reverse Transfer Capacitance	C_{RSS}	f=1.0MHz		49		pF
Switching Characteristics						
Total Gate Charge (Note 1)	Q_G	V_{DS}=20V,V_{GS}=0 to 10V,		64		nC
Gate-Source Charge	Q_{GS}	I_D=30A(NOTE1,2)		15		nC
Gate-Drain Charge	Q_{GD}			6.5		nC
Gate charge at threshold	$Q_{g(th)}$			8.1		nC
Switching charge	Q_{SW}			14		nC
Gate plateau voltage	$Q_{plateau}$			3.0		V
Gate charge total	Q_g	V_{DS}=20V,V_{GS}=0 to 4.5V, I_D=30A		31		nC
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1V,V_{GS}=0 to 10V,		60		nC
Output charge	Q_{OSS}	V_{DD}=20V,V_{GS}=0V,		40		nC
Turn-On Delay Time (Note 1)	$t_{D(ON)}$	V_{DS}=20V,V_{GS}=0 to 10V,		9.8		ns
Turn-On Rise Time	t_R	R_G=1.6Ω,I_D=30A		5.6		ns
Turn-Off Delay Time	$t_{D(OFF)}$	(NOTE1,2)		39		ns
Turn-Off Fall Time	t_F			6.2		ns
Drain-source Diode Characteristics And Maximum Ratings						
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	I_{SD}=50A,V_{GS}=0V		0.83	1.4	V
Diode continuous forward current	I_S	Tc=25°C			100	A
Reverse Recovery time	trr	V_{GS}=0V,I_{SD}=50A di/dt=100A/us		78		nS
Reverse Recovery Charge	Qrr	V_{GS}=0V,I_{SD}=50A di/dt=100A/us		90		nC

Notes:
1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

Test Circuits and waveforms

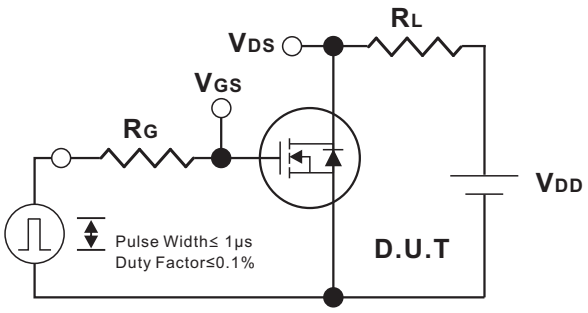


Peak Diode Recovery dv/dt Test Circuit

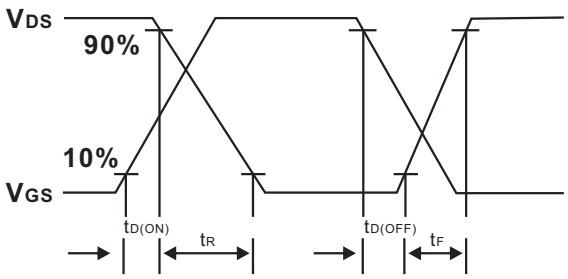


Peak Diode Recovery dv/dt Waveforms

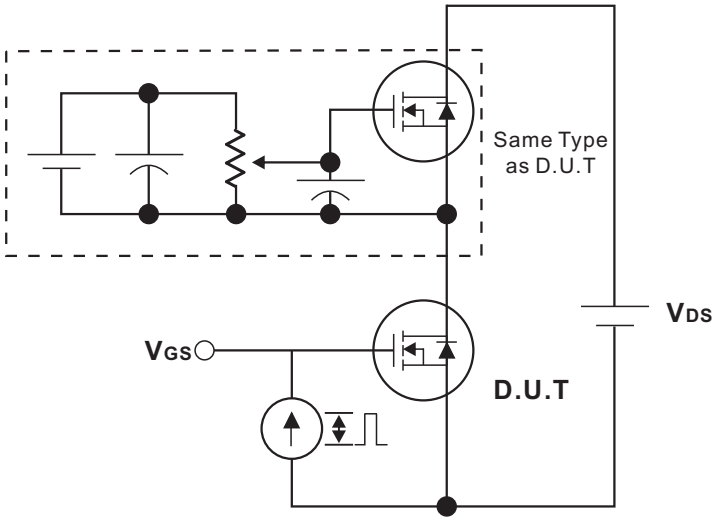
Test Circuits and waveforms



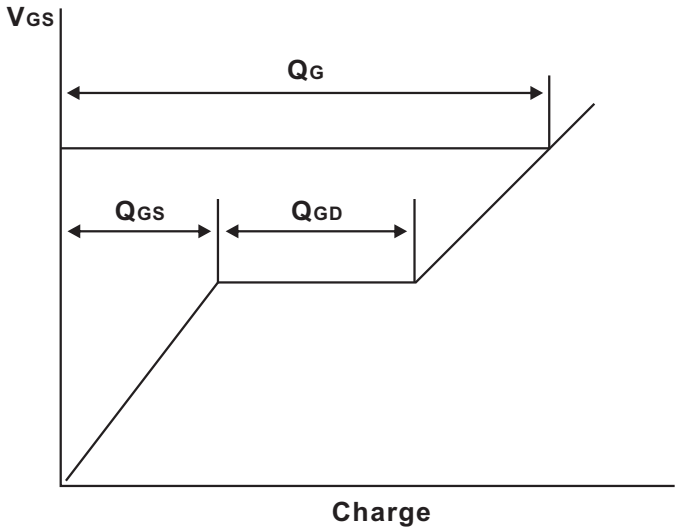
Switching Test Circuit



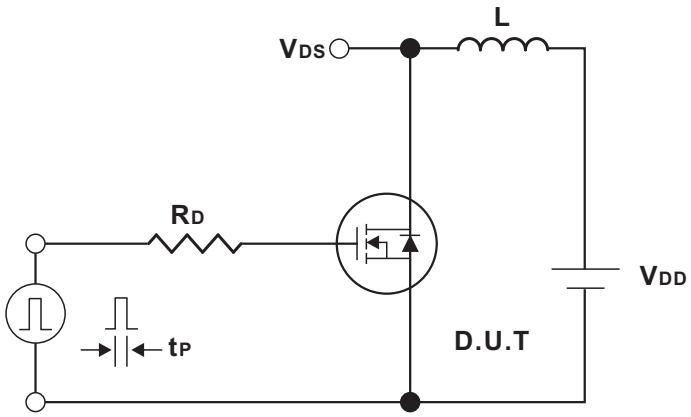
Switching Waveforms



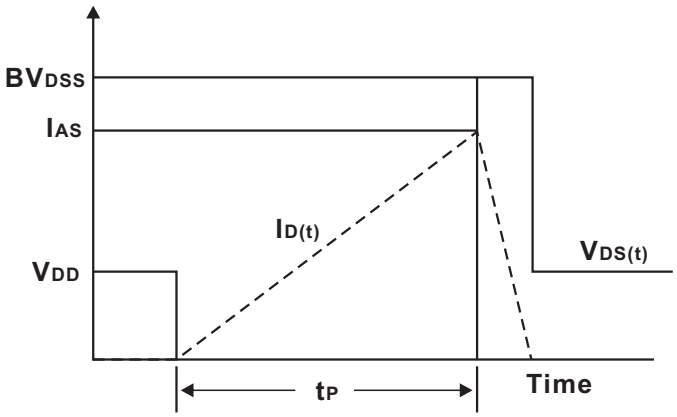
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

Typical Characteristics

Fig.1 Output Characteristics

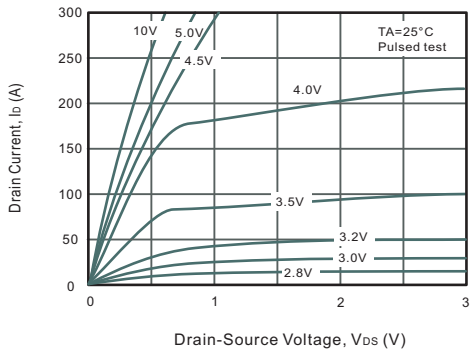


Fig.2 Transfer Characteristics

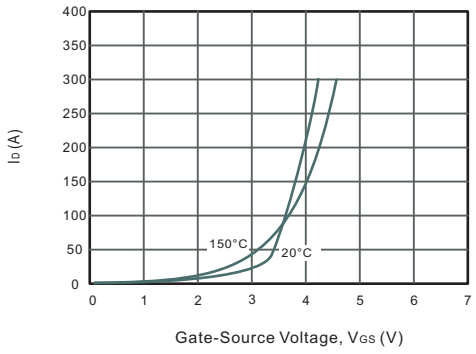


Fig.3 RDS(on) vs Drain Current and Gate Voltage

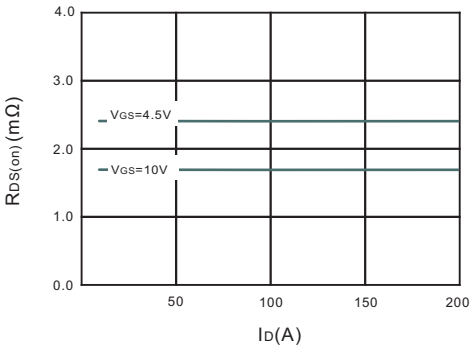


Fig.4 RDS(on) vs. Temperature

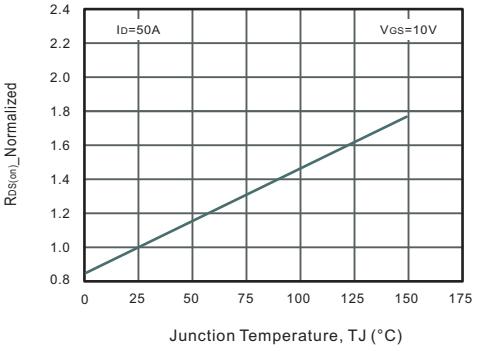


Fig.5 Typ. forward transconductance

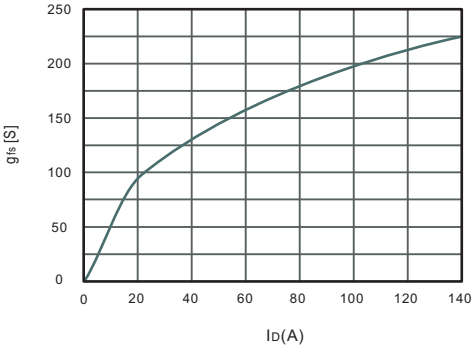


Fig.6 Capacitance Characteristics

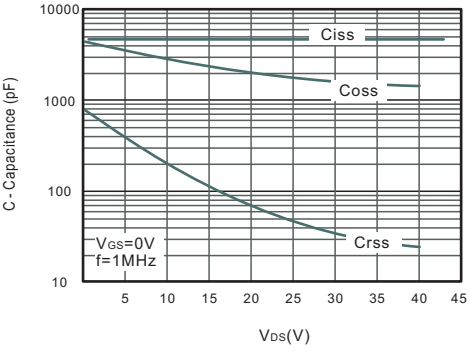


Fig.7 Gate Charge Characteristics

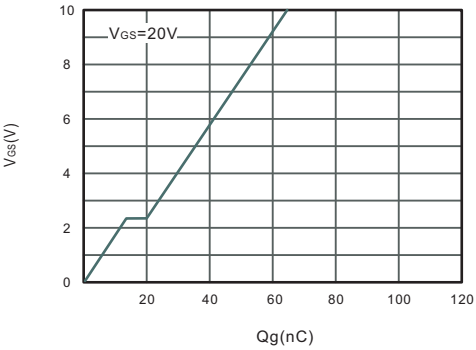
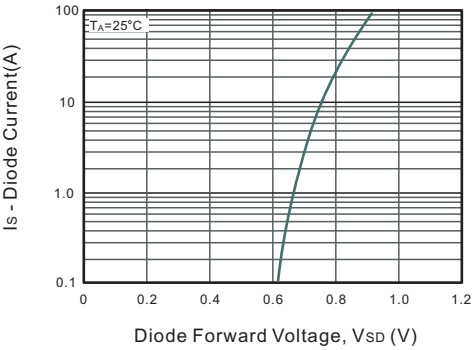


Fig.8 Body-diode Forward Characteristics



Typical Characteristics

Fig.9 Power Dissipation

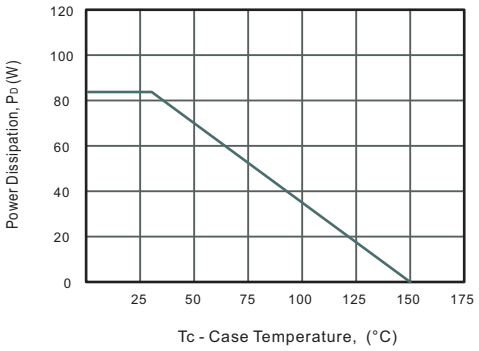


Fig.10 Drain Current Derating

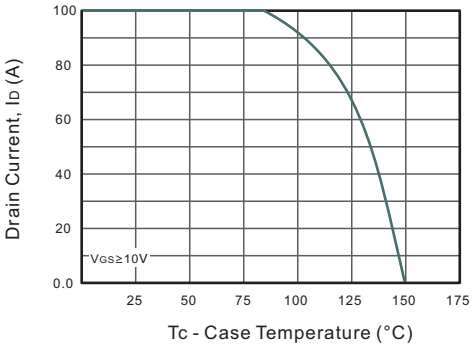


Fig.11 Safe Operating Area

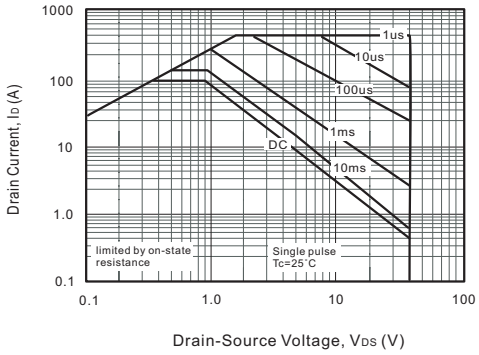


Fig.12 RGS(th) vs TJ Characteristics

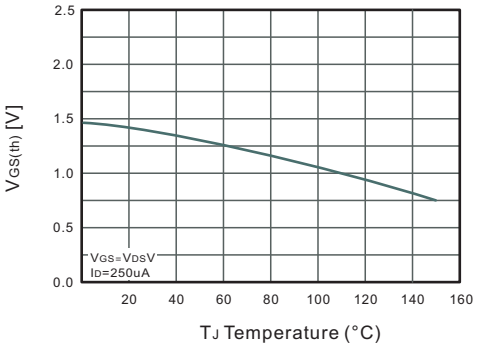
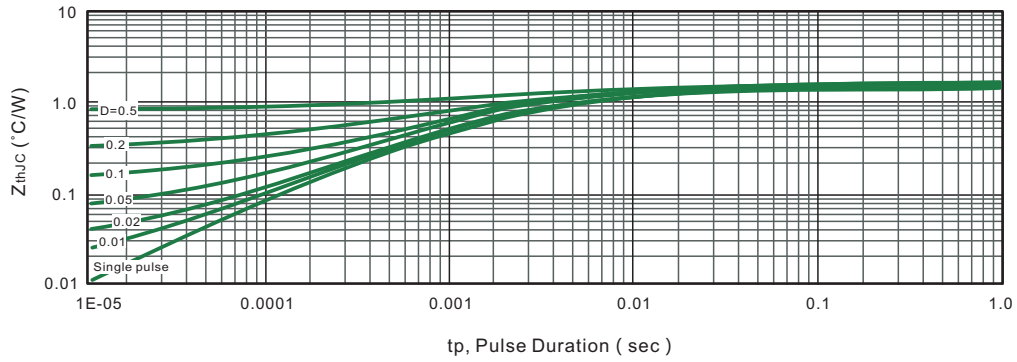
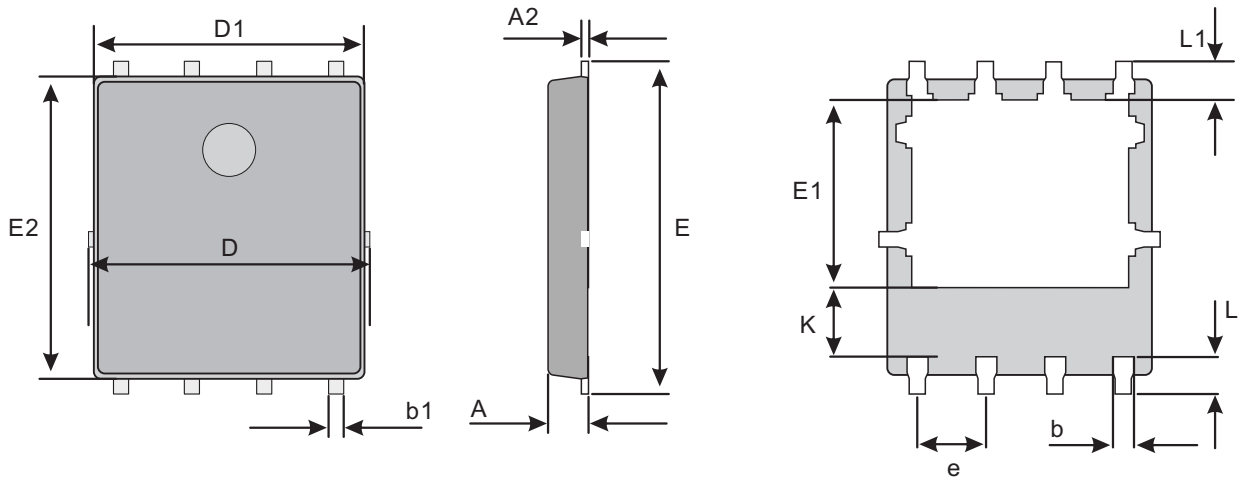


Fig.13 Max. Transient Thermal Impedance



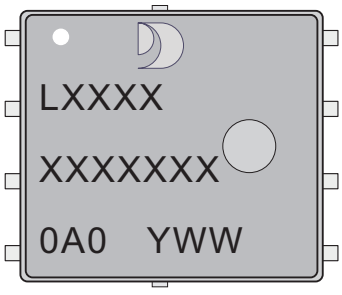
Package Outline
Plastic surface mounted package;8 leads **PDFN5060-8L**



Mechanical data

UNIT		A	A2	b	b1	D	D1	E	E1	E2	e	K	L	L1
mm	max	1.1	0.304	0.4 ref.	0.4	5.3	5.24	6.35	3.675	6.09	1.27 typ.	1.29 typ.	0.785	0.7 typ.
	typ	1.0	0.254		0.3	5.15	5.04	6.15	3.475	5.89			0.685	
	min	0.9	0.204		0.2	5.0	4.84	5.95	3.275	5.69			0.585	
mil	max	43	12	16 ref.	16	209	206	250	145	240	50 typ.	51 typ.	31	28 typ.
	typ	39	10		12	203	198	242	137	232			27	
	min	35	8		8	197	191	234	129	224			23	

Marking Diagram



Jingdao Logo
Unmarkable Surfacea
Pin1 Mark
LXXXX XXXXXXX: Marking code
0A0: Traceability code
YWW:Y: Years(0~9)
WW: Week

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