

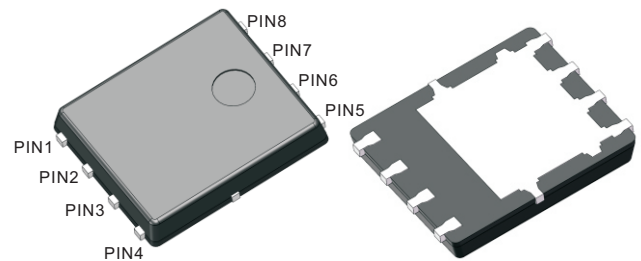


## 100A, 40V N-CHANNEL POWER MOSFET

PDFN5060-8L(Prefix :L)

### Description

This model is an n-channel enhanced MOS power field effect transistor manufactured by silicon epitaxial process. This model has excellent switching characteristics, extremely low on impedance, low gate charge and other characteristics.

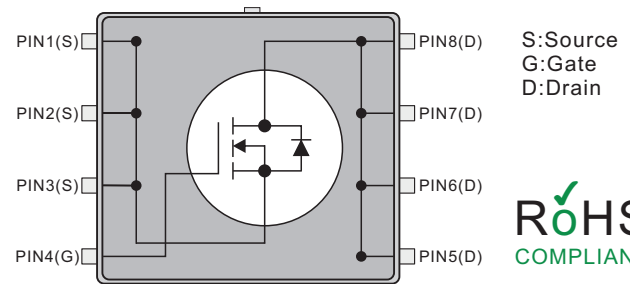


### Features

- $R_{DS(ON)} < 2.1 \text{ m}\Omega @ V_{GS}=10\text{V}, I_D=50\text{A}$
- Extremely low on impedance
- Low gate charge
- Superior switching characteristics
- 100% Avalanche tested
- 100%  $\Delta V_{DS}$  tested

### Mechanical data

- Case: PDFN5060-8L
- Approx. Weight:0.093g ( 0.0032oz)
- Lead free finish, RoHS compliant
- Case Material: "Green" molding compound, UL flammability classification 94V-0, "Halogen-free".



### Packing Marking And Ordering Information

Device Package	Device	Marking	Packing Type	QTY Per Reel	Inner box	Per Carton
PDFN5060-8L	L1R7NS40S	L1R7NS40S	Reel	5,000 Pcs	10,000 Pcs	50,000 Pcs

### Absolute Maximum Ratings (Ta=25°C, Unless Otherwise Specified)

Parameter	Symbols	Ratings	Units
Drain-Source Voltage	$V_{DSS}$	40	V
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	100	A
Pulsed Drain Current (Note 2)	$I_{DM}$	400	A
Avalanche Energy Single Pulsed (Note 3)	$E_{AS}$	264	mJ
Power Dissipation (Tc = 25°C)	$P_D$	83	W
Operating junction and storage temperature	$T_J, T_{STG}$	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.  
2. Repetitive Rating: Pulse width limited by maximum junction temperature.  
3. L = 0.5mH, IAS = 32.5A, RG = 25  $\Omega$ , Starting TJ = 25°C

### Thermal Resistance

Parameter	Symbols	Ratings	Units
Thermal resistance, junction – case.	$R_{thJC}$	1.5	°C/W
Thermal resistance, junction – ambient(min. footprint)	$R_{thJA}$	50	°C/W



Electrical Characteristics (Ta=25°C, Unless Otherwise Specified)

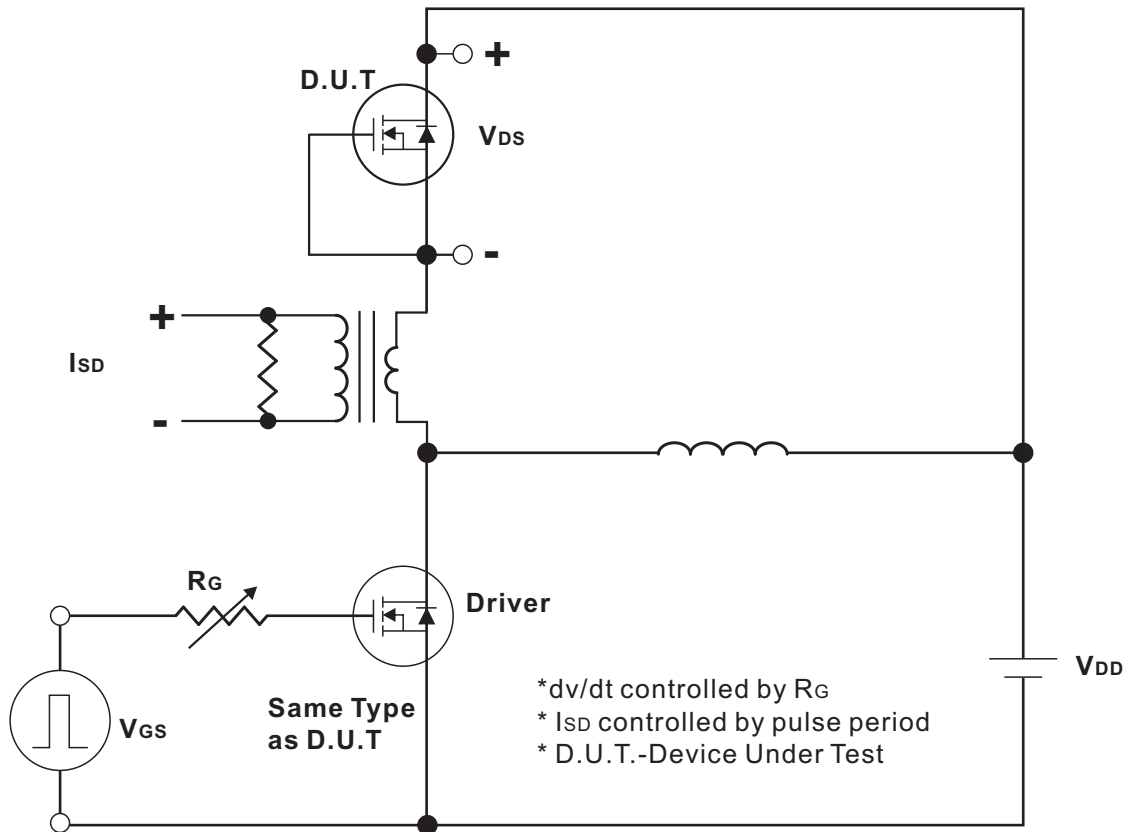
Parameter	Symbols	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	40			V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$		0.1	1.0	$\mu A$
Gate- Source Leakage Current	$I_{GSS}$	$V_{GS}=20V, V_{DS}=0V$		10	100	nA
<b>On Characteristics</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.4		2.4	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=50A$		2.4	3.0	m $\Omega$
		$V_{GS}=10V, I_D=50A$		1.7	2.1	
Gate resistance	$R_G$			1.6		$\Omega$
Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=50A$		60		S
<b>Dynamic Characteristics</b>						
Input Capacitance	$C_{ISS}$	$V_{DS}=20V,$		4766		pF
Output Capacitance	$C_{OSS}$	$V_{GS}=0V,$		1821		pF
Reverse Transfer Capacitance	$C_{RSS}$	$f=1.0MHz$		49		pF
<b>Switching Characteristics</b>						
Total Gate Charge (Note 1)	$Q_G$	$V_{DS}=20V, V_{GS}=0$ to 10V, $I_D=30A$ (NOTE1,2)		64		nC
Gate-Source Charge	$Q_{GS}$			15		nC
Gate-Drain Charge	$Q_{GD}$			6.5		nC
Gate charge at threshold	$Q_{g(th)}$			8.1		nC
Switching charge	$Q_{SW}$			14		nC
Gate plateau voltage	$Q_{plateau}$			3.0		V
Gate charge total	$Q_g$	$V_{DS}=20V, V_{GS}=0$ to 4.5V, $I_D=30A$		31		nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1V, V_{GS}=0$ to 10V,		60		nC
Output charge	$Q_{OSS}$	$V_{DD}=20V, V_{GS}=0V,$		40		nC
Turn-On Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=20V, V_{GS}=0$ to 10V, $R_G=1.6\Omega, I_D=30A$ (NOTE1,2)		9.8		ns
Turn-On Rise Time	$t_R$			5.6		ns
Turn-Off Delay Time	$t_{D(OFF)}$			39		ns
Turn-Off Fall Time	$t_F$			6.2		ns
<b>Drain-source Diode Characteristics And Maximum Ratings</b>						
Drain-Source Diode Forward Voltage (Note 1)	$V_{SD}$	$I_{SD}=50A, V_{GS}=0V$		0.83	1.4	V
Diode continuous forward current	$I_S$	$T_C=25^\circ C$			100	A
Reverse Recovery time	$t_{rr}$	$V_{GS}=0V, I_{SD}=50A$ $di/dt=100A/\mu s$		78		ns
Reverse Recovery Charge	$Q_{rr}$	$V_{GS}=0V, I_{SD}=50A$ $di/dt=100A/\mu s$		90		nC

Notes:

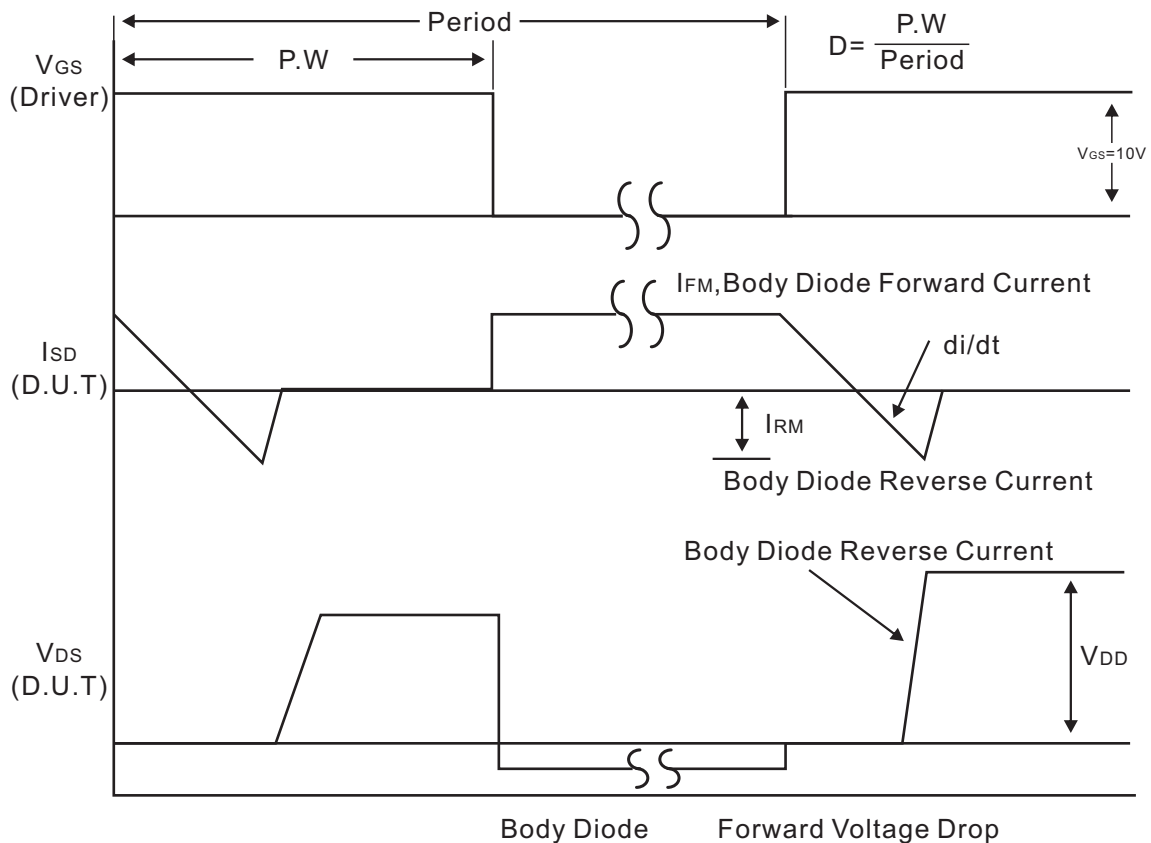
1. Pulse Test: Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ .
2. Essentially independent of operating temperature.



Test Circuits and waveforms



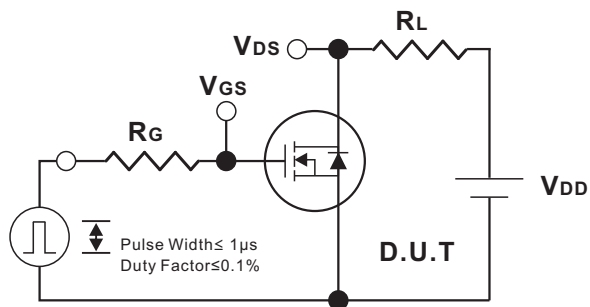
Peak Diode Recovery dv/dt Test Circuit



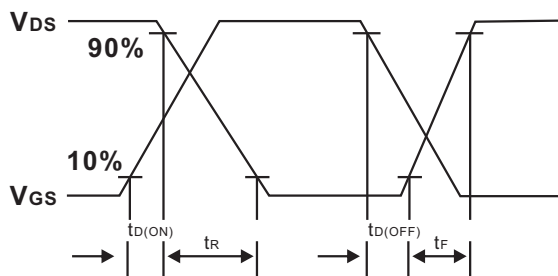
Peak Diode Recovery dv/dt Waveforms



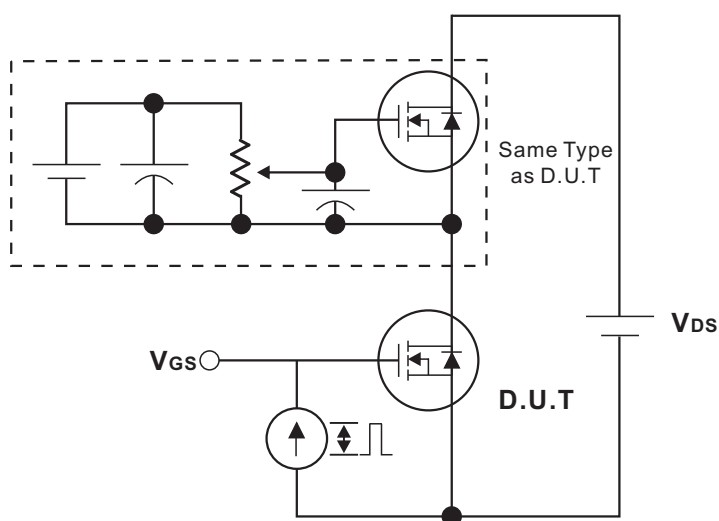
### Test Circuits and waveforms



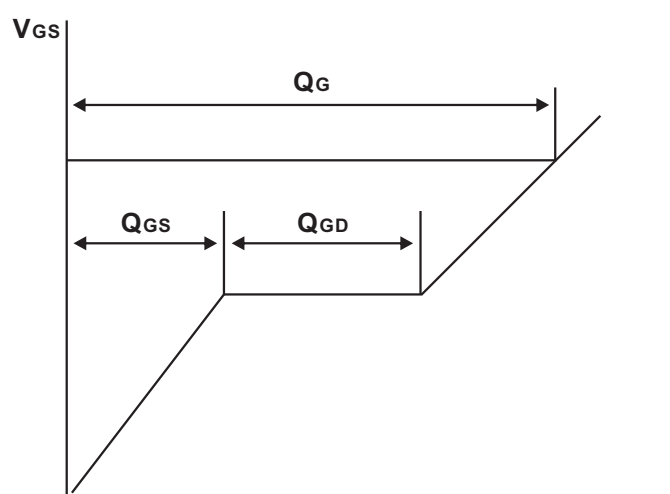
Switching Test Circuit



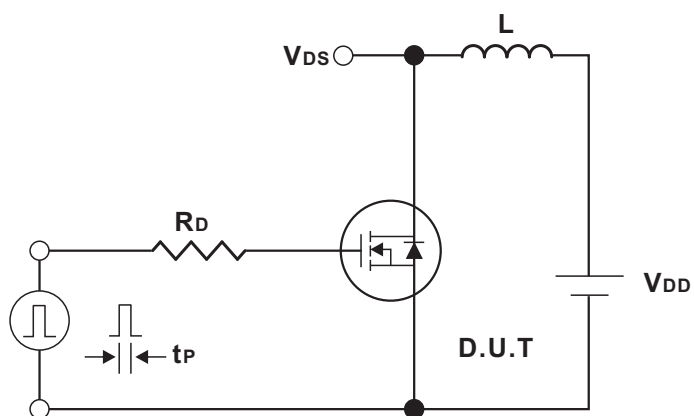
Switching Waveforms



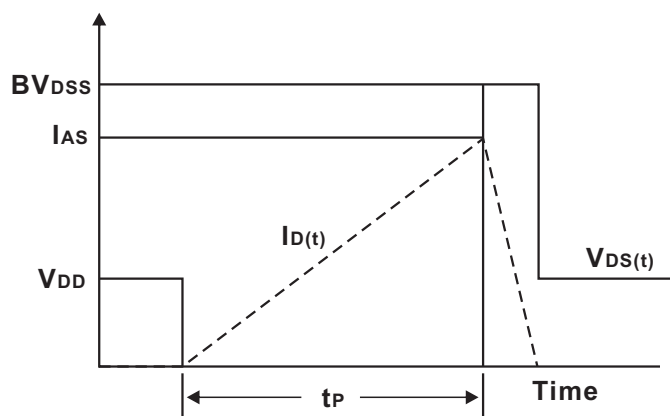
Gate Charge Test Circuit



Charge  
Gate Charge Waveform



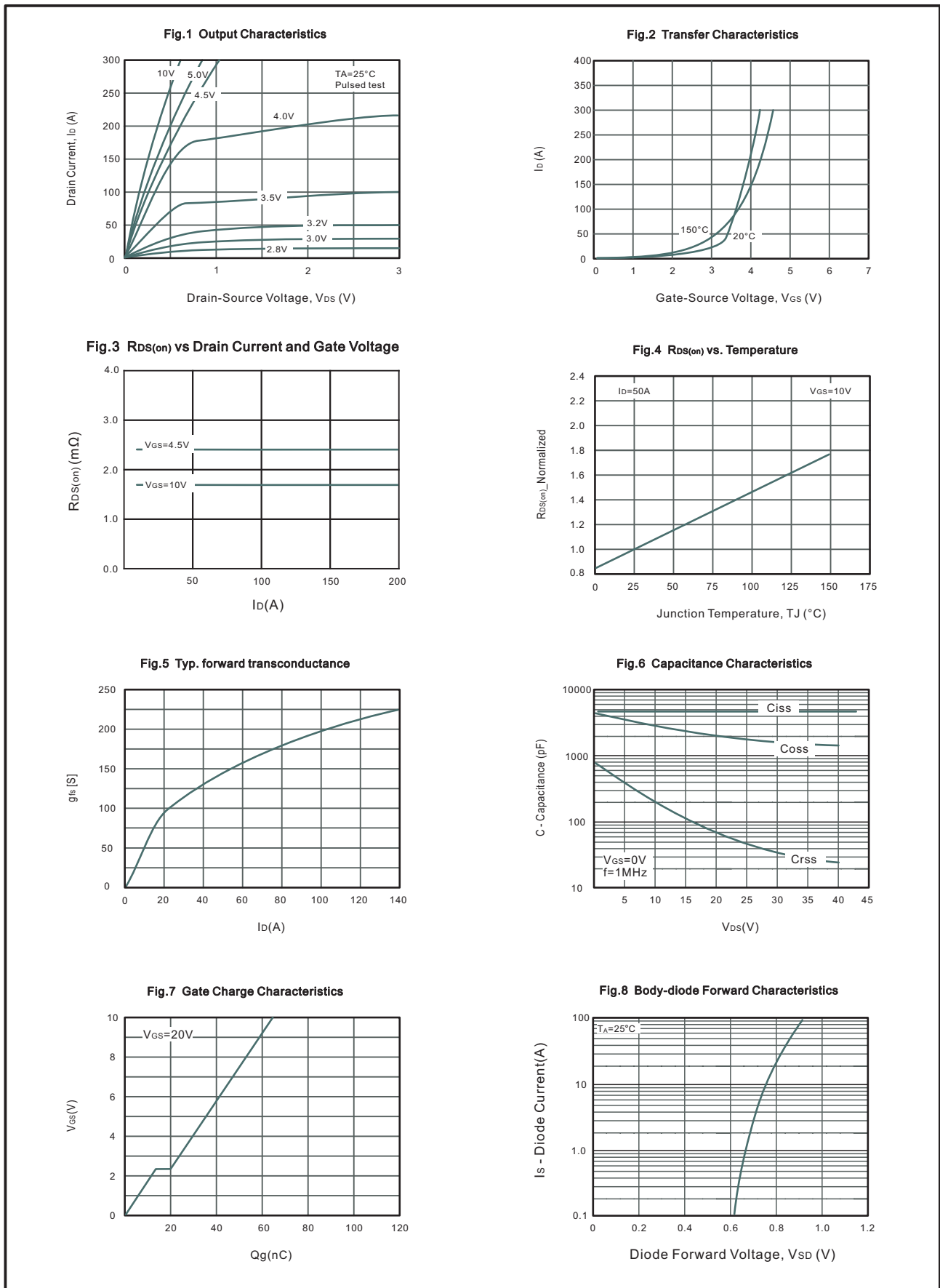
Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms



### Typical Characteristics





### Typical Characteristics

Fig.9 Power Dissipation

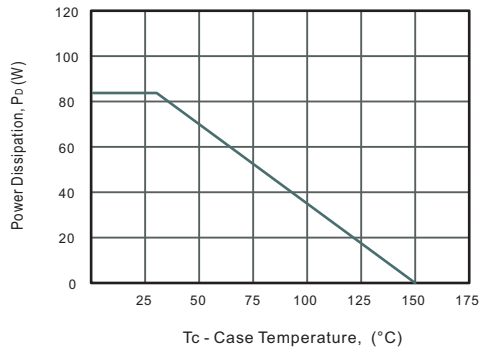


Fig.10 Drain Current Derating

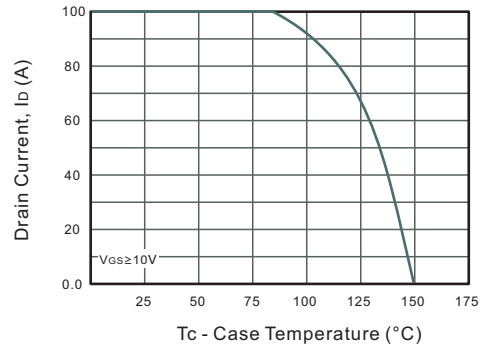


Fig.11 Safe Operating Area

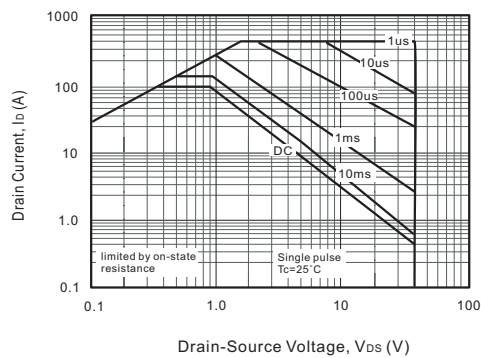


Fig.12  $R_{GS(th)}$  vs  $T_J$  Characteristics

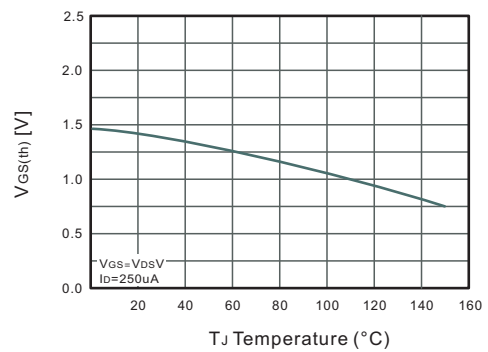
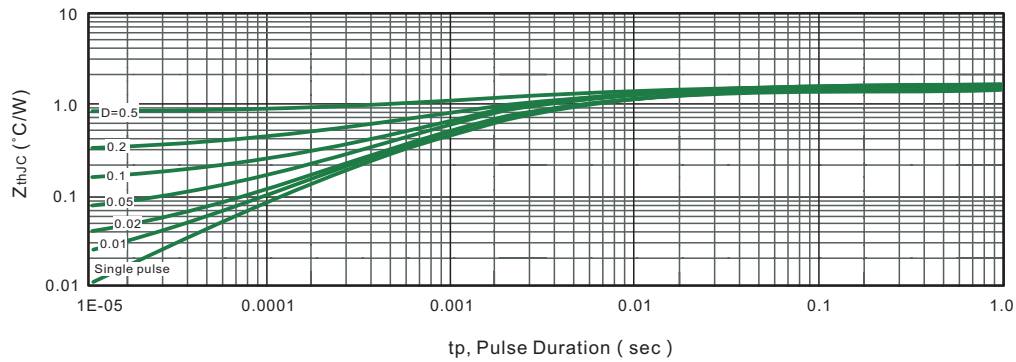


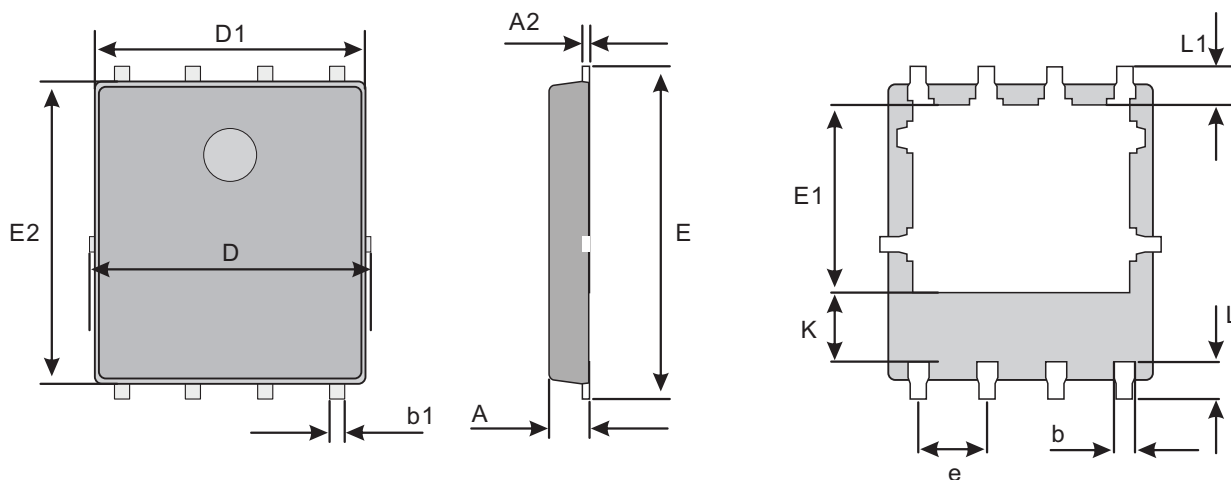
Fig.13 Max. Transient Thermal Impedance





Package Outline  
Plastic surface mounted package;8 leads

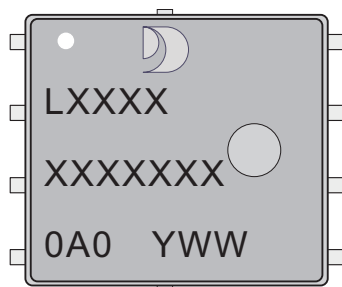
PDFN5060-8L



Mechanical data

UNIT		A	A2	b	b1	D	D1	E	E1	E2	e	K	L	L1
mm	max	1.1	0.304	0.4 ref.	0.4	5.3	5.24	6.35	3.675	6.09	1.27 typ.	1.29 typ.	0.785	0.7 typ.
	typ	1.0	0.254		0.3	5.15	5.04	6.15	3.475	5.89			0.685	
	min	0.9	0.204		0.2	5.0	4.84	5.95	3.275	5.69			0.585	
mil	max	43	12	16 ref.	16	209	206	250	145	240	50 typ.	51 typ.	31	28 typ.
	typ	39	10		12	203	198	242	137	232			27	
	min	35	8		8	197	191	234	129	224			23	

Marking Diagram



- Jingdao Logo
- Unmarkable Surfacea
- Pin1 Mark
- LXXXX XXXXXXXX: Marking code
- 0A0: Traceability code
- YWW: Y: Years(0~9)
- WW: Week



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